REMARKS

Rejection of claims 15, 20 and 23 under 35 U.S.C. §101

The examiner rejected claims 15, 20 and 23 under 35 U.S.C. §101. Claims 15, 20 and 23 have been amended to recite recordable media, and claims 16-17, 21-22 and 24-25 have been cancelled. Applicant respectfully asserts that claims 15, 20 and 23 as amended, which are limited to recordable media, recite statutory subject matter under 35 U.S.C. §101, and respectfully request reconsideration of the examiner's rejection of claims 15, 20 and 23 in light of the amendments herein.

Rejection of claims 1-27 under 35 U.S.C. §102(b)

The examiner rejected claims 1-27 under 35 U.S.C. §102(b) as being anticipated by Jeddeloh. In rejecting claim 1, the examiner states Jeddeloh teaches a database query processor residing in the memory and executed by the at least one processor, citing col. 3 lines 62-67 and col. 4 lines 1-5 of Jeddeloh. The cited language in Jeddeloh refers to FIG. 1, which shows a hardware configuration for a computer system. The language at col. 3 lines 62-67 states:

> The embodiment illustrated in FIG. 1 operates as follows in processing a read memory request. First, a processor, such as processor 112, performs a read operation. This read operation is relayed across processor bus 108 into one of memory controllers 122 and 123 within north bridge 102. Consider the case where the read request is directed to memory controller 122. Memory controller 122 issues the read request to memory 104. In response to this read request, memory 104 returns the read data to memory controller 122. Next, the read operation is completed by transferring data across processor bus 108 to processor 112.

The memory controllers 122 and 123 in Jeddeloh are hardware components, and thus do not read on a database query processor in claim 1 that resides in the memory and is

executed by one or more processors. For this reason, Jeddeloh does not teach or suggest the database query processor recited in claim 1.

In the rejection of claim 1, the examiner goes on to state that Jeddeloh teaches the database query processor processing a first query to generate a first result set by interrogating a database, and, if a second query may be satisfied by the first result set, generating a second result set from the first result set without caching the first result set and without interrogating the database for the second query, citing col. 3 lines 62-67 and col. 5 lines 15-51. This rejection suffers from many problems. First, the examiner provides no detailed mapping of the teachings of Jeddeloh on the many limitations listed in the recited claim limitation. For example, what teaching in Jeddeloh reads on the first result set in claim 1? What teaching in Jeddeloh reads on the second result set in claim 1? What teaching in Jeddeloh reads on generating a second result set from the first result set without caching the first result set and without interrogating the database for the second query? Because Jeddeloh does not clearly teach these limitations, and because the examiner has not identified any teachings in Jeddeloh that allegedly read on these limitations, the examiner has failed to establish a prima facie case of anticipation for claim 1 under 35 U.S.C. §102(b).

Another problem with the examiner's rejection of claim 1 is equating hardware components in a memory system to the software components in the claims. While memory holds data and a database hold data, it is well-understood in the art that a memory is not a database. Claim 1 specifically recites at least one processor, a memory, and a database query processor residing in the memory and executed by the at least one processor. Claim 1 thus clearly recites a database query processor that is software. A hardware memory controller in Jeddeloh simply does not read on a software database query processor under 35 U.S.C. §102(b).

Even if we assume at a theoretical level that the examiner's application of Jeddeloh to claim 1 is correct (which it is not for the reasons given above), the memory controller in Jeddeloh does not teach all of the limitations in claim 1. The language cited by the examiner at col. 5 lines 15-51 of Jeddeloh discusses FIG. 4. This method in FIG. 4 assures data coherency in a system that includes multiple memory controllers. Because memory requests may be received by the two memory controllers, the access by the two memory controllers to the memory must be coordinated to assure one of the memory controllers does not corrupt data in memory that is being accessed by the other memory controller. The method in FIG. 4 assures data coherency between the two memory controllers by using source tags to identify the source of a memory request. If the second memory controller contains pending memory requests from the same source as requests in the first memory controller, the first memory controller is stalled until the pending requests are complete, as shown in step 406 in FIG. 4 of Jeddeloh. The memory request is then issued to RAM in step 408. The function represented in FIG. 4 of Jeddeloh is summarized in the Abstract of Jeddeloh:

> The apparatus also includes a request order enforcement circuit that is configured to prevent the memory request from issuing from the first memory controller before the pending memory requests from the same source within the second memory controller complete.

We see from the plain language in Jeddeloh that the issue being addressed is data coherency by serializing accesses to memory by the same source. In Jeddeloh, all accesses to memory are still made to memory. The main issue in Jeddeloh is assuring the memory accesses to memory are made in the proper order. Every memory access in Jeddeloh is eventually made to the memory. Some may be stalled to wait for earlier accesses to complete, but all of the memory accesses in Jeddeloh eventually are made to memory. This feature of Jeddeloh expressly teaches away from the limitations in claim 1 that recite "generating a second result set from the first result set without caching the first result set and without interrogating the database for the second query." In claim 1, if a second query may be satisfied by the first result set that resulted from interrogating a

database, the second result set may be generated from the first result set without interrogating the database. For the examiner's rejection to have any merit, a first request from a memory controller in Jeddeloh would result in a first result set, and a second request from the memory controller would then have to cause the generation of a second result set from the first result set without the second request accessing memory. However, this is not consistent with the express teachings in Jeddeloh. In Jeddeloh, every memory access accesses the memory. Thus, there is no teaching in Jeddeloh that reads on generating a second result set from a first result set without interrogating the database for the second query, as expressly recited in claim 1.

Because Jeddeloh teaches hardware memory controllers that do not reside in memory and are not executed by one or more processors, the hardware memory controllers in Jeddeloh do not read on the database query processor in claim 1. Because every memory access in Jeddeloh accesses memory, Jeddeloh teaches away from generating a second result set for a second query from a first result set without interrogating the database for the second query. As a result, claim 1 is allowable over Jeddeloh, and applicants respectfully request reconsideration of the examiner's rejection of claim 1 under 35 U.S.C. §102(b).

In rejecting claim 2, the examiner recites all of the many limitations in claim 2, then simply cites to col. 5, lines 15-51 of Jeddeloh as allegedly teaching these many limitations. Because there are no teachings in the cited portion of Jeddeloh that clearly read on the limitations in claim 2, and because the examiner has not provided any mapping of the teachings of Jeddeloh on the limitations in claim 2, the examiner has failed to establish a prima facie case of anticipation for claim 2 under 35 U.S.C. §102(b). Jeddeloh teaches serializing memory accesses by hardware memory controllers to assure data coherency. Nowhere does Jeddeloh teach or suggest using a first result set from a first query to generate at least one other result set for at least one other query, as recited in claim 2. For this reason, claim 2 is allowable over Jeddeloh. In addition, claim 2

depends in claim 1, which is allowable for the reasons given above. As a result, claim 2 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 2 under 35 U.S.C. §102(b).

In rejecting claim 3, the examiner states that col. 5 lines 15-51 of Jeddeloh teaches a database query processor that generates a new query for each group that will produce a result set that will satisfy all queries in the group, processes each new query, and generates from the result set of each new query at least one other result set for queries in the group corresponding to the new query. Yet the examiner has not specifically mapped the teachings of Jeddeloh on these many limitations in claim 3. What teaching in Jeddeloh reads on the new query in claim 3? What teaching in Jeddeloh reads on the result set in claim 3 that satisfies all queries in a group? What teaching in Jeddeloh reads on generating from the result set of each new query at least one other result set? Because the examiner has not mapped the teachings of Jeddeloh on these many limitations in claim 3, the examiner has failed to establish a prima facie case of anticipation for claim 3 under 35 U.S.C. §102(b). Jeddeloh teaches ordering memory accesses. Nowhere does Jeddeloh teach or suggest creating a new memory access that could correspond to the new query in claim 3. Nowhere does Jeddeloh teach or suggest a result set that will satisfy all queries in a group. Nowhere does Jeddeloh teach or suggest generating from the result set of each new query at least one other result set for queries in the group corresponding to the new query. As a result, claim 3 is allowable over Jeddeloh. In addition, claim 3 depends in claim 1, which is allowable for the reasons given above. As a result, claim 3 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 3 under 35 U.S.C. §102(b).

Claim 4 includes limitations similar to those in claims 1 and 2 that were addressed above, and is therefore allowable for the same reasons. Applicants respectfully request reconsideration of the examiner's rejection of claim 4 under 35 U.S.C. §102(b).

Claim 5 includes limitations similar to those in claims 1 and 3 that were addressed above, and is therefore allowable for the same reasons. Applicants respectfully request reconsideration of the examiner's rejection of claim 5 under 35 U.S.C. §102(b).

In rejecting claim 6, the examiner states that Jeddeloh teaches "wherein the database processor delays processing the plurality of received queries for a predetermined time period", citing col. 2 lines 4-41 of Jeddeloh. While the cited language in Jeddeloh does teach delaying some memory accesses until others can be completed, this does not read on delaying processing the plurality of received queries for a predetermined time period, as recited in claim 6. The time period in Jeddeloh is variable, depending on the number of pending memory accesses, and therefore does not read on "a predetermined time period" as recited in claim 6. For this reason, claim 6 is allowable over Jeddeloh. In addition, claim 6 depends in claim 5, which is allowable for the reasons given above. As a result, claim 6 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 6 under 35 U.S.C. §102(b).

In rejecting claim 7, the examiner states that Jeddeloh teaches "wherein the database query processor delays processing the plurality of received queries until a predetermined number of the plurality of the queries has been received", citing col. 2 lines 4-41 of Jeddeloh. In Jeddeloh, pending memory accesses in two different memory controllers are ordered to assure data coherency. Nowhere does Jeddeloh teach or suggest delaying the processing of memory accesses until a predetermined number of memory accesses has been received. To the contrary, the delaying in Jeddeloh depends on the number of potentially conflicting memory accesses that happen to be pending at a given

time. Thus, at one time in Jeddeloh there may be two conflicting memory accesses, which results in one of them being delayed. At another time in Jeddeloh there may be six conflicting memory accesses, which results in five of them being delayed. This shows that Jeddeloh expressly teaches away from delaying processing of memory accesses until a predetermined number of memory accesses have been received. For these reasons, claim 7 is allowable over Jeddeloh. In addition, claim 7 depends in claim 5, which is allowable for the reasons given above. As a result, claim 7 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 7 under 35 U.S.C. §102(b).

Claim 8 is a method claim that includes limitations similar to those in claim 1 that was addressed above, and is therefore allowable for the same reasons. Applicants respectfully request reconsideration of the examiner's rejection of claim 8 under 35 U.S.C. §102(b).

Claim 9 includes limitations similar to those in claims 1 and 2 that were addressed above, and is therefore allowable for the same reasons. In addition, claim 9 depends in claim 8, which is allowable for the reasons given above. As a result, claim 9 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 9 under 35 U.S.C. §102(b).

Claim 10 includes limitations similar to those in claims 1 and 3 that were addressed above, and is therefore allowable for the same reasons. In addition, claim 10 depends in claim 8, which is allowable for the reasons given above. As a result, claim 10 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 10 under 35 U.S.C. §102(b).

Claim 11 is a method claim that includes limitations similar to those in claim 4 that was addressed above, and is therefore allowable for the same reasons. Applicants respectfully request reconsideration of the examiner's rejection of claim 11 under 35 U.S.C. §102(b).

Claim 12 is a method claim that includes limitations similar to those in claim 5 that was addressed above, and is therefore allowable for the same reasons. Applicants respectfully request reconsideration of the examiner's rejection of claim 12 under 35 U.S.C. §102(b).

Claim 13 is a method claim that includes limitations similar to those in claim 6 that was addressed above, and is therefore allowable for the same reasons. In addition, claim 13 depends in claim 12, which is allowable for the reasons given above. As a result, claim 13 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 13 under 35 U.S.C. §102(b).

Claim 14 is a method claim that includes limitations similar to those in claim 7 that was addressed above, and is therefore allowable for the same reasons. In addition, claim 14 depends in claim 12, which is allowable for the reasons given above. As a result, claim 14 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 14 under 35 U.S.C. §102(b).

Claim 15 is a program product claim that includes limitations similar to those in claim 1 that was addressed above, and is therefore allowable for the same reasons. Applicants respectfully request reconsideration of the examiner's rejection of claim 15 under 35 U.S.C. §102(b).

Claims 16 and 17 have been cancelled herein, and therefore need not be addressed.

Claim 18 includes limitations similar to those in claims 1 and 2 that were addressed above, and is therefore allowable for the same reasons. In addition, claim 18 depends in claim 15, which is allowable for the reasons given above. As a result, claim 18 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 18 under 35 U.S.C. §102(b).

Claim 19 includes limitations similar to those in claims 1 and 3 that were addressed above, and is therefore allowable for the same reasons. In addition, claim 19 depends in claim 15, which is allowable for the reasons given above. As a result, claim 19 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 19 under 35 U.S.C. §102(b).

Claim 20 is a program product claim that includes limitations similar to those in claim 4 that was addressed above, and is therefore allowable for the same reasons. Applicants respectfully request reconsideration of the examiner's rejection of claim 20 under 35 U.S.C. §102(b).

Claims 21 and 22 have been cancelled herein, and therefore need not be addressed.

Claim 23 is a program product claim that includes limitations similar to those in claim 5 that was addressed above, and is therefore allowable for the same reasons. Applicants respectfully request reconsideration of the examiner's rejection of claim 23 under 35 U.S.C. §102(b).

Claims 24 and 25 have been cancelled herein, and therefore need not be addressed.

Claim 26 is a program product claim that includes limitations similar to those in claim 6 that was addressed above, and is therefore allowable for the same reasons. In addition, claim 26 depends in claim 23, which is allowable for the reasons given above. As a result, claim 26 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 26 under 35 U.S.C. §102(b).

Claim 27 is a program product claim that includes limitations similar to those in claim 7 that was addressed above, and is therefore allowable for the same reasons. In addition, claim 27 depends in claim 23, which is allowable for the reasons given above. As a result, claim 27 is also allowable as depending on an allowable independent claim. Applicants respectfully request reconsideration of the examiner's rejection of claim 27 under 35 U.S.C. §102(b).

Conclusion

In summary, Jeddeloh does not teach, support, or suggest the unique combination of features in applicants' claims presently on file. Therefore, applicants respectfully assert that all of applicants' claims are allowable. Such allowance at an early date is respectfully requested. The Examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this case.

Respectfully submitted,

By /derekpmartin
Derek P. Martin
Reg. No. 36,595

MARTIN & ASSOCIATES, L.L.C.
P.O. Box 548
Carthage, MO 64836-0548
(417) 358-4700